What is claimed is:

1. A capacitor comprising:

a plurality of conductive layers embedded in a dielectric; and

a plurality of vias coupling at least two of the plurality of conductive layers to a plurality of connection sites.

2. The capacitor of claim 1, wherein the capacitor has a thickness of between about .5 millimeter and about 1 millimeter.

3. The capacitor of claim 2, wherein the capacitor has a capacitance of between about 20 and about 30 microfarads.

4. The capacitor of claim 1, wherein the plurality of controlled collapse chip connection sites have a pitch of between about 100 and about 500 microns.

5. The capacitor of claim 1, wherein the plurality of vias are plated through holes.

6. A capacitor comprising:

a plurality of first conductive layers;

a plurality of second conductive layers interlaced with the plurality of first conductive layers;

a number of surfaces having a plurality of connection sites operable for coupling the capacitor to a substrate using a controlled collapse chip connection (C4); and

a plurality of vias coupling the plurality of first conductive layers and the plurality of second conductive layers to at least two of the plurality of connection sites.

7. The capacitor of claim 6, wherein each of the plurality of first conductive layers is fabricated from a tungsten paste.

8. The capacitor of claim 6, wherein the number of surfaces is two.

9. A capacitor comprising:

a multilayered capacitor having a number of outer surfaces; and

a number of pads located on at least two of the number of outer surfaces wherein at least two of the number of pads are capable of being coupled to a substrate using a solder bump.

10. The capacitor of claim 9, wherein the multilayered capacitor includes a number of parallel conductive layers and the number of pads are coupled to the number of parallel conductive layers through vias.

11. The capacitor of claim 10, wherein the number of conductive layers is greater than about 50.

12. The capacitor of claim 11, wherein the number of pads is greater than about 4000.

13. A system comprising:

a die including an electronic system;

a capacitor located less than about .1 millimeter from the die and coupled to the die, the capacitor is capable of decoupling a power supply connection at the die without additional capacitors located external to the die; and

a dielectric layer located between the capacitor and the die.

14. The system of claim 13, wherein the dielectric layer has a thickness of between about .05 millimeters and about .1 millimeters.

15. A system comprising:

a first die;

a second die; and

a capacitor having a first surface having a controlled collapse chip connection coupled to the first die and a second surface having a controlled collapse chip connection coupled to the second die.

16. The system of claim 15, wherein the first die includes a processor and the second die includes a communication system.

17. A system comprising:

a substrate having a surface; and

a capacitor having a plurality of vias coupled to a plurality of conductive layers in the capacitor, the capacitor is coupled to the surface at a plurality of connection sites.

18. A system comprising:

a substrate having a first surface and a second surface;

a die coupled to the first surface; and

a capacitor having a plurality of vias coupled to a plurality of conductive layers in the capacitor, the capacitor is coupled to the second surface by a controlled collapse chip connection and the capacitor is electrically coupled to the die through the substrate.

19. The system of claim 18, wherein the die includes a processor.

20. The system of claim 19, wherein the die has a die surface and the capacitor has a capacitor surface and the capacitor surface is located less than about .1 millimeter from the die surface.

21. A system comprising:

a processor requiring at least 5 watts of power to be operable; and

a single multilayered single package capacitor coupled to the processor and capable of decoupling a power supply from the processor.

22. The system of claim 21, wherein the single multilayered single package capacitor is capable of being mounted on a substrate by a plurality of solder bumps.

23. The system of claim 22, wherein the single multilayered capacitor is capable of being mounted on a substrate using a controlled collapse chip connection.

24. A method comprising:
forming a stack of a plurality of screen printed dielectric sheets;
forming a plurality of via holes in the stack;
filling at least two of the plurality of via holes with a metal slurry; and
co-firing the stack to form a capacitor.

25. The method of claim 24, further comprising:
coupling the stack to a substrate using a controlled collapse chip connection.

26. The method of claim 24, further comprising:
coupling a die to the substrate and to the capacitor.

27. A method comprising:
forming a capacitor having a plurality of conductive layers and a surface; and
forming a pattern of pads on the surface, at least one pad in the pattern of pads is capable of being coupled to at least one of the plurality of conductive layers and capable of being coupled to a substrate using a solder bump attachment.

28. The method of claim 27, further comprising:
coupling the capacitor to a ceramic substrate using a solder bump attachment.

29. A method comprising:
selecting a substrate having a controlled collapse chip connection capability; and

mounting a multilayered capacitor on the substrate using the controlled collapse chip connection capability.